AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 7, line 10, with the following amended paragraph.

A first embodiment of the present invention will be explained with reference to the accompanying drawings. In this embodiment, the present invention has been adapted to an electronic control unit (ECU) 1 loaded to a vehicle. Fig. 1 is a block diagram of a structure of a microcomputer of this first embodiment. A microcomputer 2 is formed as a single chip. The microcomputer 2 is provided, as a basic structure, with a CPU 3 which operates depending on programs, a ROM 5 for previously storing programs and fixed data and a RAM ~~7~~6 for temporarily storing a result of arithmetic operation executed by the CPU 3. Moreover, the ECU 1 is provided, as a control object, for example, with an indicator lamp and an actuator, while the microcomputer 2 is provided with an I/O port 7 for an actuator or the like.

Please replace the paragraph beginning on page 15, line 23, with the following amended paragraph.

In addition, the timer time can be set freely with ~~a~~ software without any limitation on the flexibility. Moreover, since measurement is realized continuously for a longer period while the CPU 3 is operated periodically, it is possible to change as required the processes during the measurement. For example, if situation changes after the measurement of timer time is started and thereby the operation assumed to be implemented is no longer required, it is possible to detect such condition to execute the other processes. For example, stability of operation of the microcomputer 2 can be confirmed by periodically checking the data or the like within the RAM ~~7~~6 and thereby reliability is improved.

Please replace the paragraph beginning on page 18, line 2, with the following amended paragraph.

The microcomputer 2 comprises an intermittent operation control section 150 and a level detecting circuit 170. The intermittent operation control section 150 is structured to input a rise request WD from the level detecting circuit 170 in addition to the intermittent operation control section ~~15~~150 of the first embodiment. The level detecting circuit 170 operates depending on a command from the CPU 3 to perform, for every constant period, the process to read the signal level via an I/O port 70 from a terminal of the microcomputer 2. The intermittent operation control section 150 and level detecting circuit 170 operate by receiving a sub-clock which is always generated from a sub-oscillation circuit 19. The level detecting circuit 170 corresponds to the automatic signal reading means and the oscillation control section 11 and intermittent control section ~~15~~150 correspond to a timer rise control means.

Please replace the paragraph beginning on page 18, line 18, with the following amended paragraph.

The CPU 3 can stop the operation thereof by executing a particular operation stop instruction. Thereby, the CPU 3 issues, when it stops the operation thereof by itself with execution of the operation stop instruction, an operation request RQ to the intermittent operation control section ~~15~~150.

Please replace the paragraph beginning on page 29, line 27, with the following amended paragraph.

The timer interlocking control section 120 is provided with a register 120a which is stored by the CPU 3. To this register 120a, a time Tq until the output of the drive signal RQ to the external apparatus 50 from reception of the operation command SD from the CPU 3 is set.

When the timer interlocking control section 120 receives the operation command SD from the CPU 3, it outputs the drive signal RQ to the external apparatus 50 via the I/O port ~~5~~ 7 after the setting time Tq being stored to the register 120a has passed. This setting time is set to such a period in which the CPU 3 will perform the operations for the predetermined number of times after it has started the intermittent operation. A preparation time Tp until the end of preparation for process of the external apparatus 50 from output of the drive signal RQ is obtained previously from the experiments. The setting time Tq is usually set to such a time in which the external apparatus 50 completes the preparation for process when the CPU 3 rises to the operating condition from the stop condition. This setting time Tq is measured on the basis of the number of sub-clocks (namely, the frequency thereof).